Abstract

Method and apparatus for soft bit computation with a reduced state equalizer. The method assures that the number of states in the equalizer is reduced to obtain acceptable complexity, while also ensuring that soft bit computation is performed for substantially all bits. The method involves computing a first set of soft bits from bits transmitted in a received signal, using a reduced-state trellis with finite non-zero delay, calculating hard decisions in response to the received signal, and also ensuring that substantially all soft bits are computed by employing zero-delay soft decision-making or decision-feedback equalization to compute a second set of soft bits. Furthermore, the hard decisions are used to compute the second set.